Spin Locks and Contention

Companion slides for The Art of Multiprocessor Programming by Maurice Herlihy & Nir Shavit

Focus so far: Correctness and Progress

- Models
 - Accurate (we never lied to you)
 - But idealized (so we forgot to mention a few things)
- Protocols
 - Elegant
 - Important
 - But naïve

New Focus: Performance

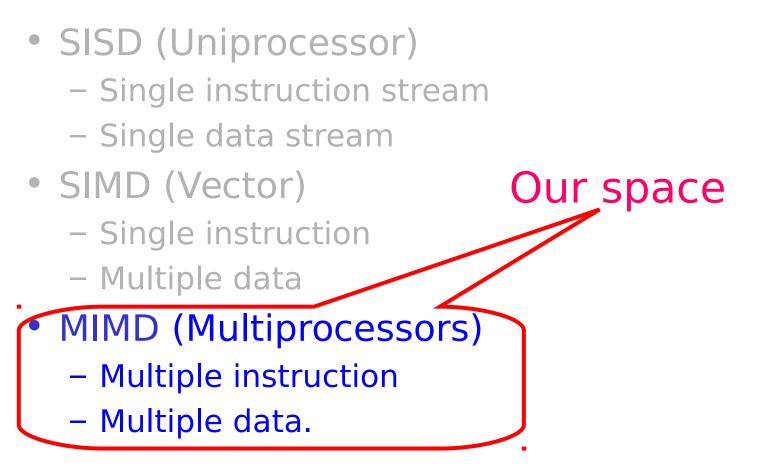
Models

- More complicated (not the same as complex!)
- Still focus on principles (not soon obsolete)
- Protocols
 - Elegant (in their fashion)
 - Important (why else would we pay attention)
 - And realistic (your mileage may vary)

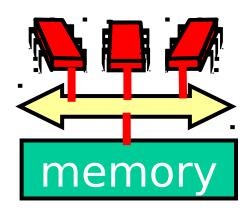
Kinds of Architectures

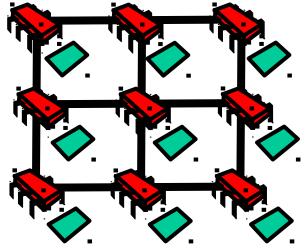
- SISD (Uniprocessor)
 - Single instruction stream
 - Single data stream
- SIMD (Vector)
 - Single instruction
 - Multiple data
- MIMD (Multiprocessors)
 - Multiple instruction
 - Multiple data.

Kinds of Architectures



MIMD Architectures





Shared Bus

Distributed

- Memory Contention
- Communication

Contention

Communication Latency

Art of Multiprocessor Programming

Today: Revisit Mutual Exclusion

- Think of performance, not just correctness and progress
- Begin to understand how performance depends on our software properly utilizing the multiprocessor machine's hardware
- And get to know a collection of locking algorithms...

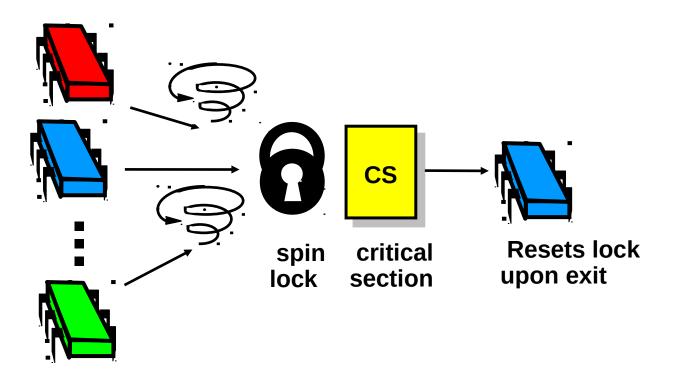
What Should you do if you can't get a lock?

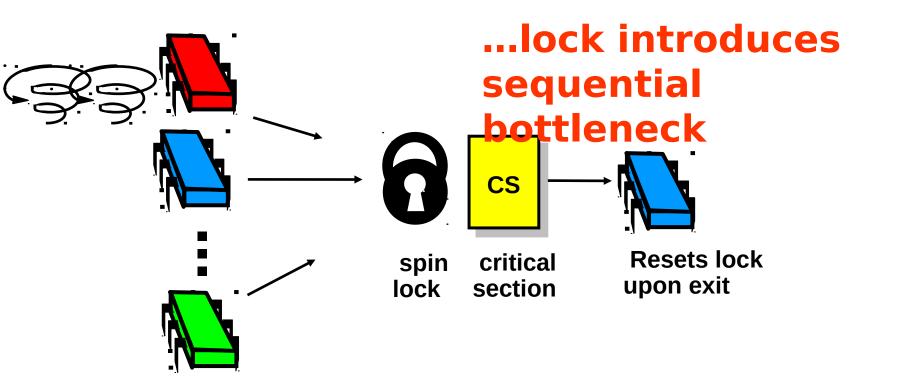
- Keep trying
 - "spin" or "busy-wait"
 - Good if delays are short
- Give up the processor
 - Good if delays are long
 - Always good on uniprocessor

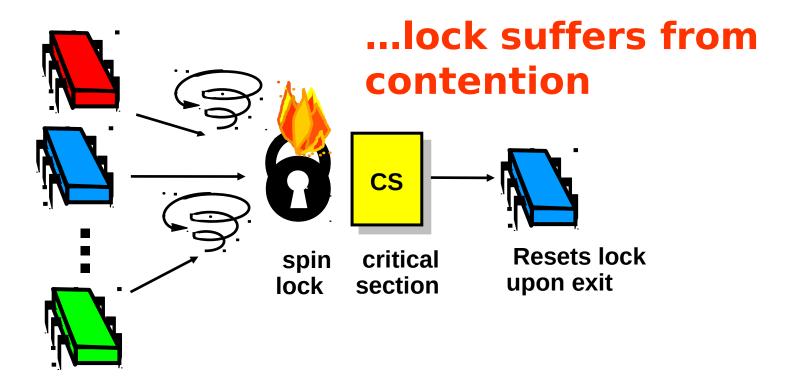
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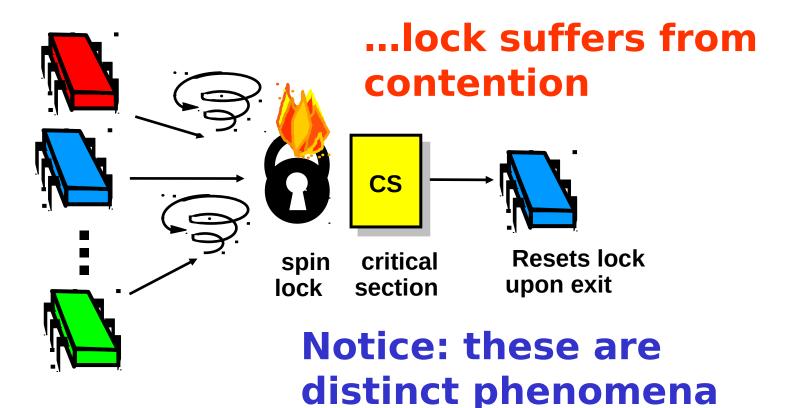
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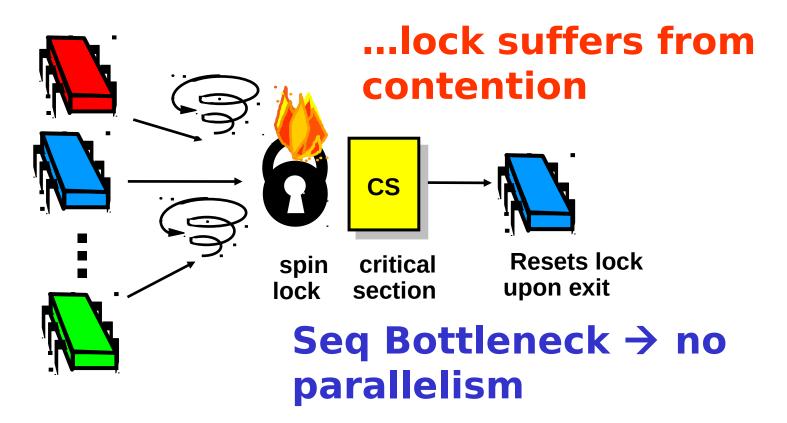
our focus

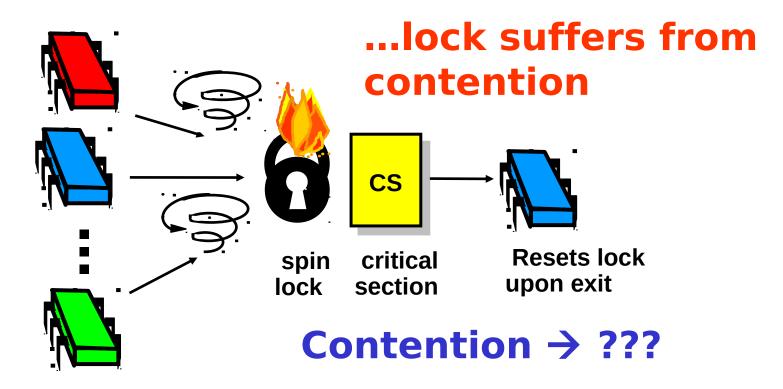








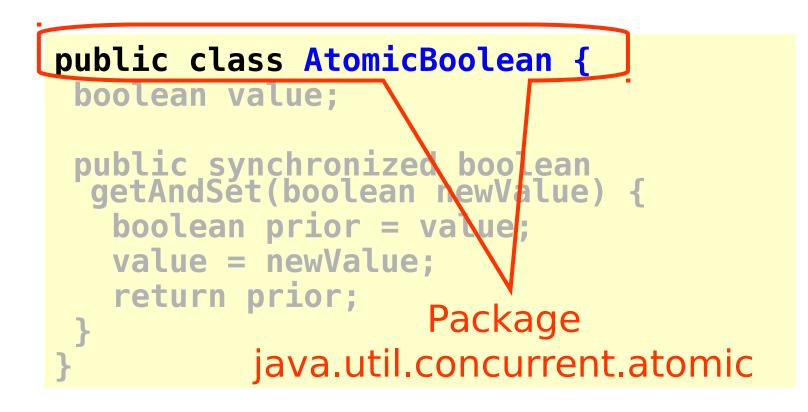




- Boolean value
- Test-and-set (TAS)
 - Swap true with current value
 - Return value tells if prior value was true or false
- Can reset just by writing false
- TAS aka "getAndSet"

```
public class AtomicBoolean {
   boolean value;

   public synchronized boolean
   getAndSet(boolean newValue) {
     boolean prior = value;
     value = newValue;
     return prior;
   }
}
```



public class AtomicBoolean {
 boolean value;

public synchronized boolean
getAndSet(boolean newValue) {
 boolean prior = value;
 value = newValue;
 return prior;

Swap old and new values

AtomicBoolean lock
 = new AtomicBoolean(false)
...
boolean prior = lock.getAndSet(true)

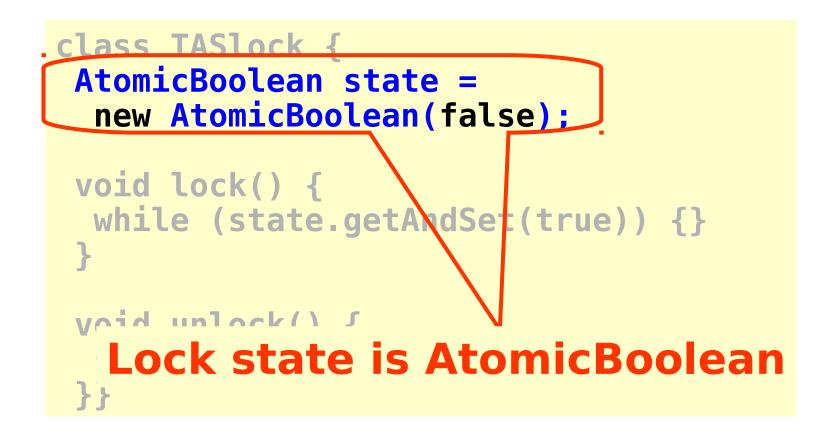
AtomicBoolean lock
 = new AtomicBoolean(false)

boolean prior = lock.getAndSet(true)

Swapping in true is called "test-and-set" or TAS

- Locking
 - Lock is free: value is false
 - Lock is taken: value is true
- Acquire lock by calling TAS
 - If result is false, you win
 - If result is true, you lose
- Release lock by writing false

```
class TASlock {
AtomicBoolean state =
  new AtomicBoolean(false);
 void lock() {
 while (state.getAndSet(true)) {}
 }
void unlock() {
  state.set(false);
 }
```



class TASlock {
 AtomicBoolean state =
 new AtomicBoolean(false);

while (state.getAndSet(true)) {}
}

Keep trying until lock acquired

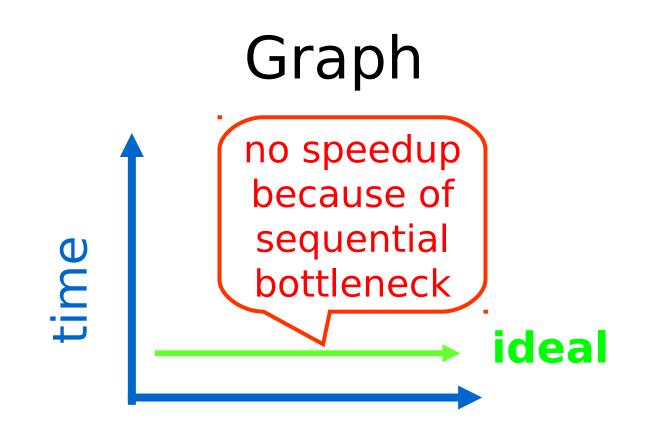


Space Complexity

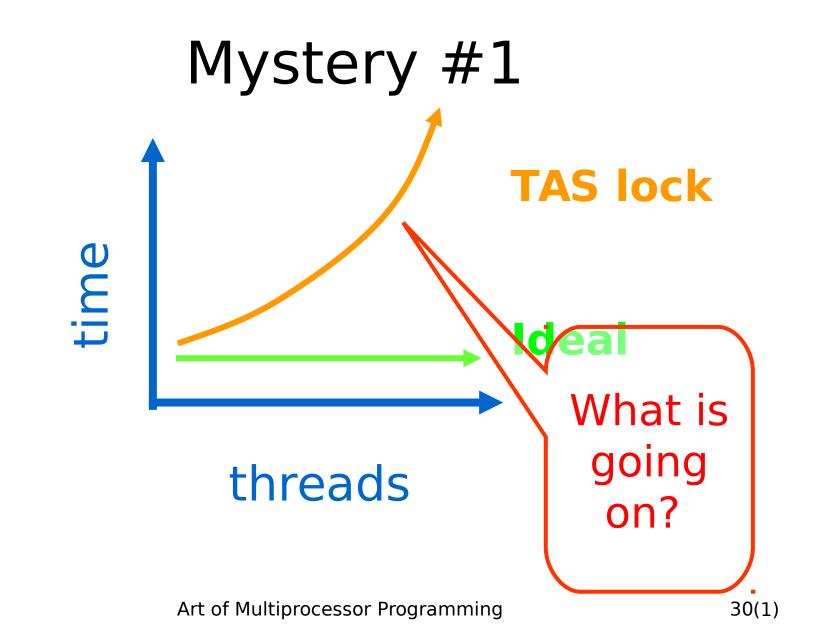
- TAS spin-lock has small "footprint"
- N thread spin-lock uses O(1) space
- As opposed to O(n) Peterson/Bakery
- How did we overcome the Ω(n) lower bound?
- We used a RMW operation...

Performance

- Experiment
 - n threads
 - Increment shared counter 1 million times
- How long should it take?
- How long does it take?



threads



Test-and-Test-and-Set Locks

- Lurking stage
 - Wait until lock "looks" free
 - Spin while read returns true (lock taken)
- Pouncing state
 - As soon as lock "looks" available
 - Read returns false (lock free)
 - Call TAS to acquire lock
 - If TAS loses, back to lurking

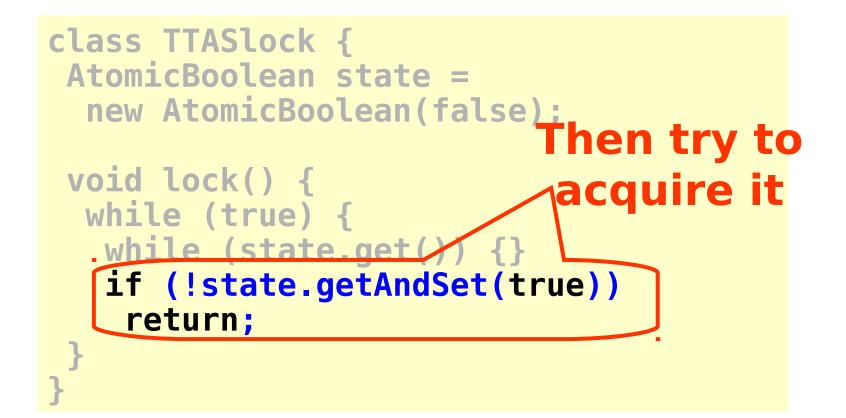
Test-and-test-and-set Lock

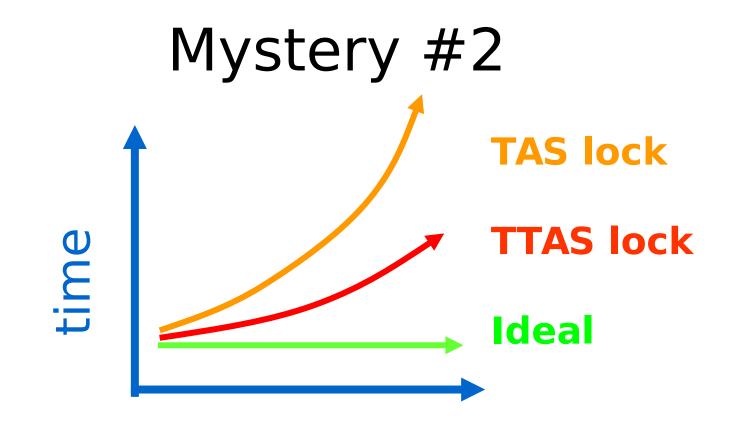
```
class TTASlock {
 AtomicBoolean state =
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 void lock() {
  while (true) {
  while (state.get()) {}
   if (!state.getAndSet(true))
    return;
```

Test-and-test-and-set Lock



Test-and-test-and-set Lock





threads

Art of Multiprocessor Programming

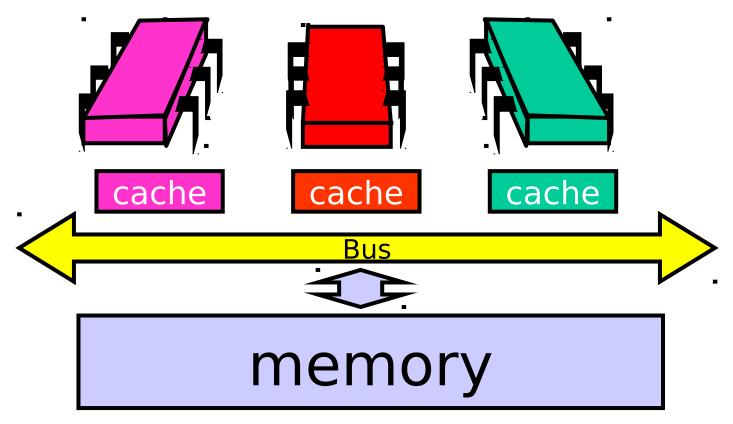
Mystery

- Both
 - TAS and TTAS
 - Do the same thing (in our model)
- Except that
 - TTAS performs much better than TAS
 - Neither approaches ideal

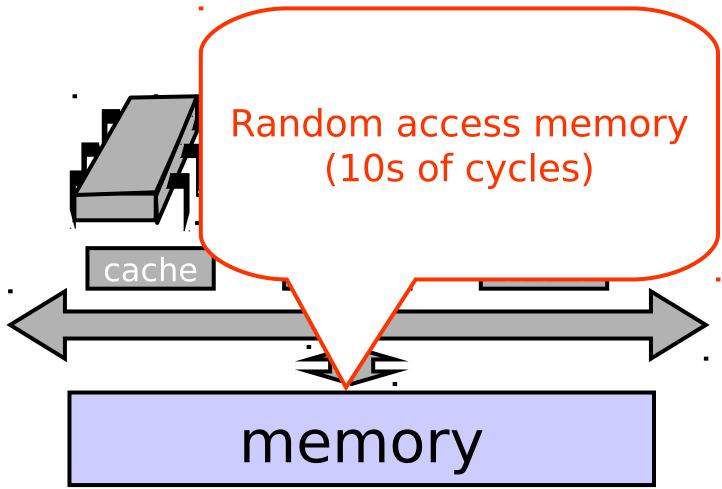
Opinion

- Our memory abstraction is broken
- TAS & TTAS methods
 - Are provably the same (in our model)
 - Except they aren't (in field tests)
- Need a more detailed model ...

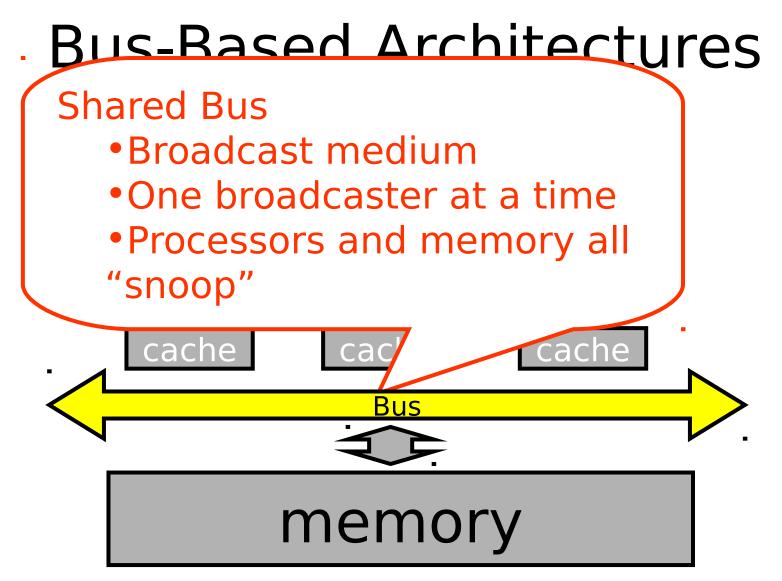
Bus-Based Architectures

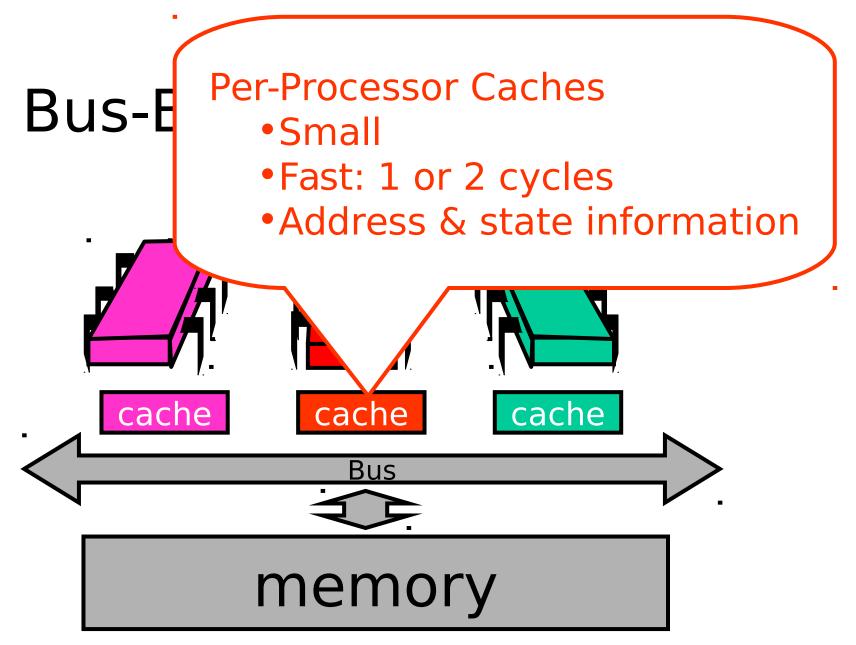


Bus-Based Architectures



Art of Multiprocessor Programming





Art of Multiprocessor Programming

Jargon Watch

- Cache hit
 - "I found what I wanted in my cache"
 - Good Thing™

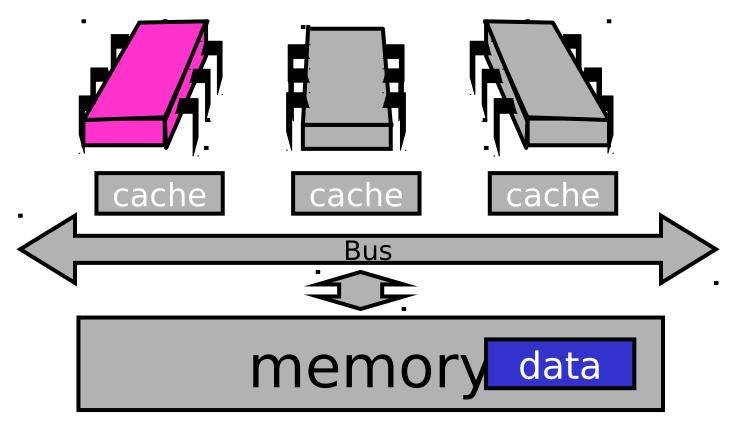
Jargon Watch

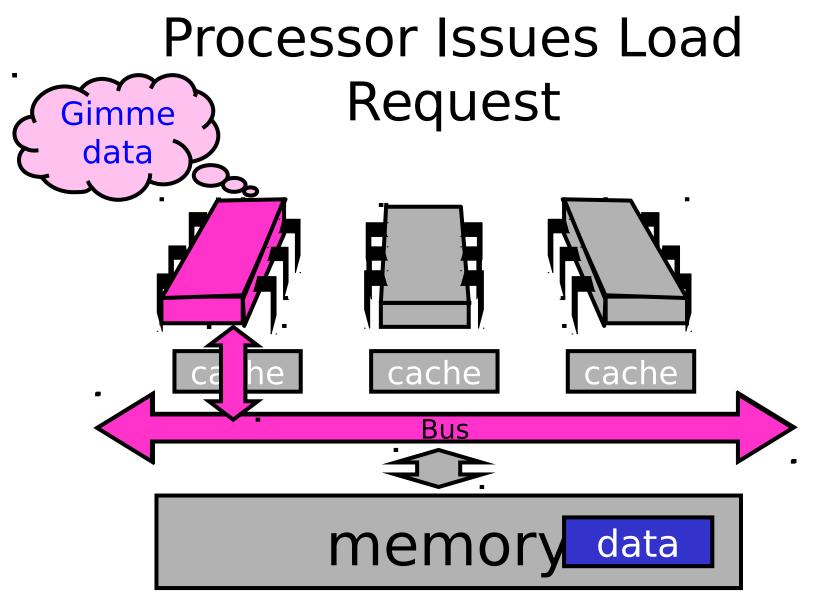
- Cache hit
 - "I found what I wanted in my cache"
 - Good Thing™
- Cache miss
 - "I had to shlep all the way to memory for that data"
 - Bad Thing™

Cave Canem

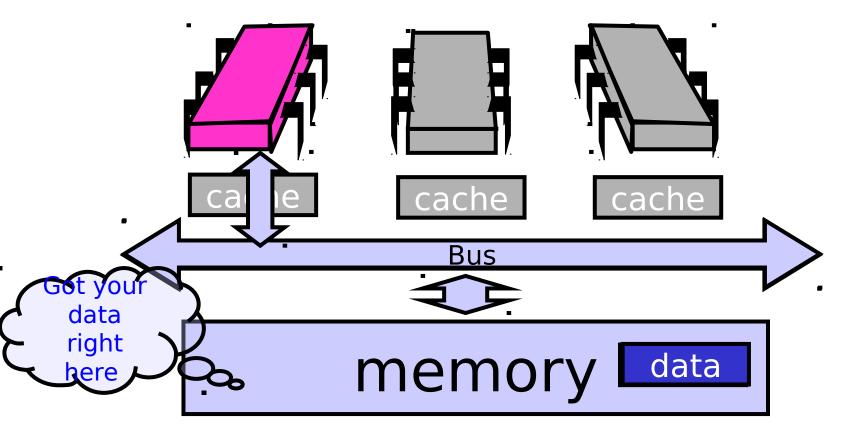
- This model is still a simplification
 - But not in any essential way
 - Illustrates basic principles
- Will discuss complexities later

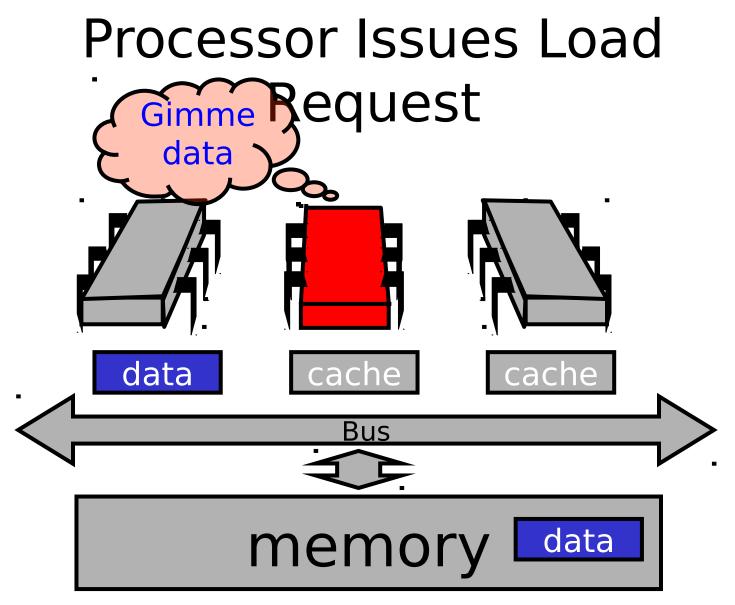
Processor Issues Load Request

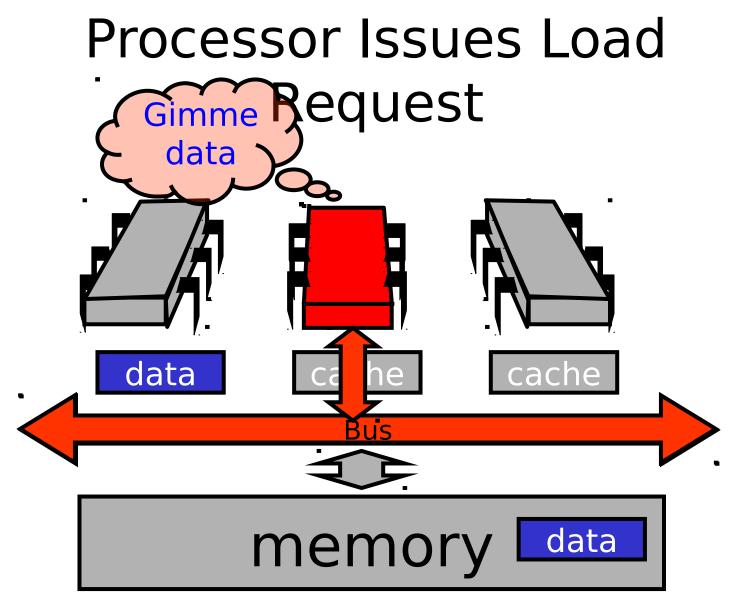


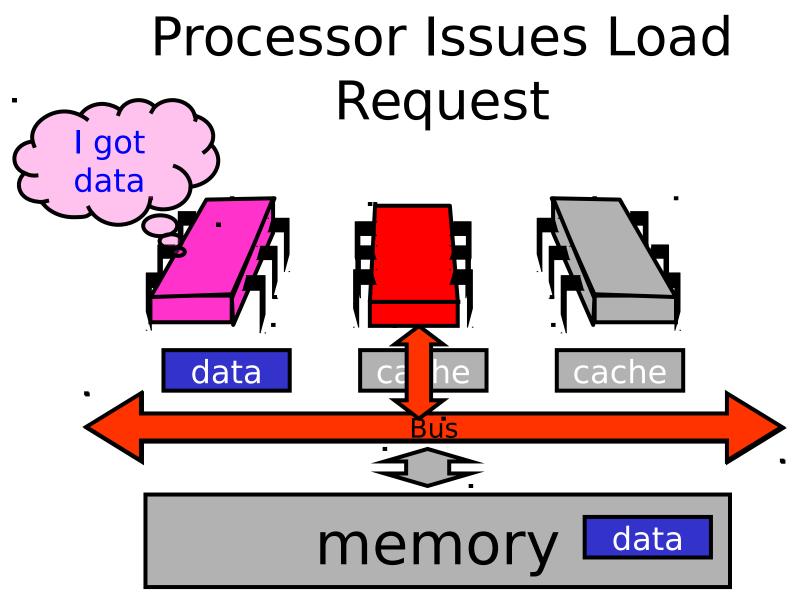


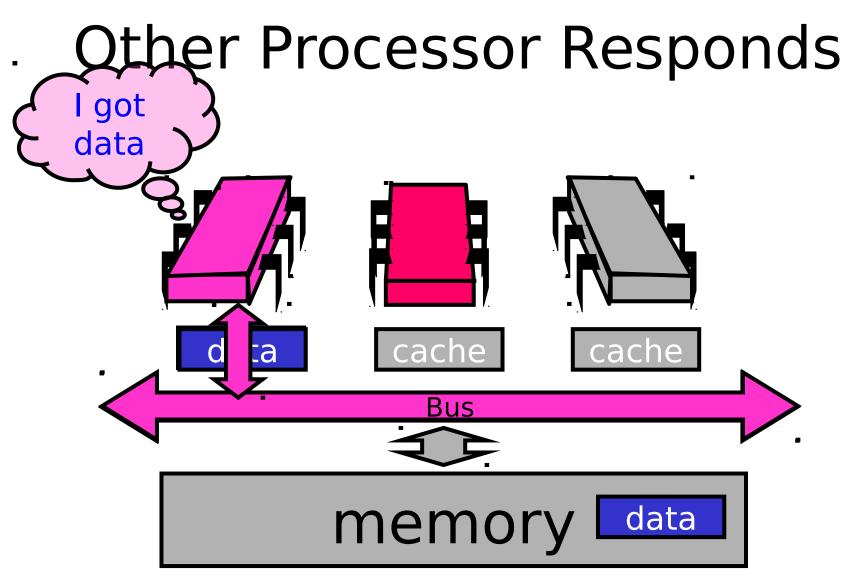
Memory Responds



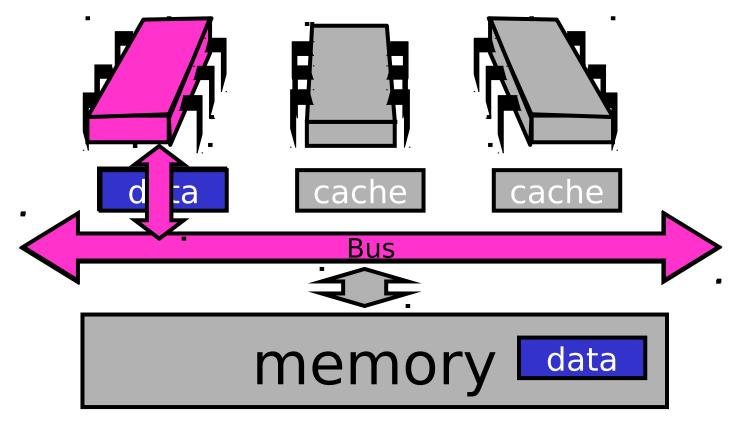


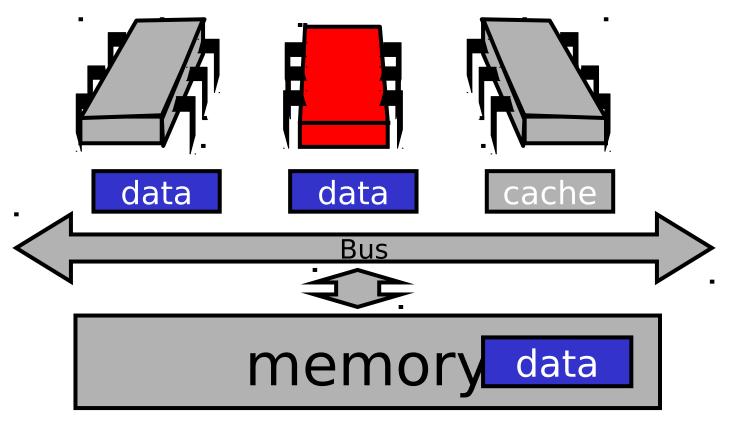


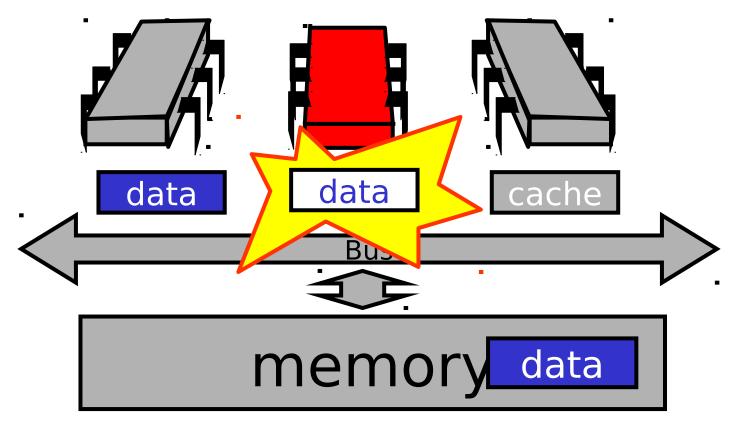


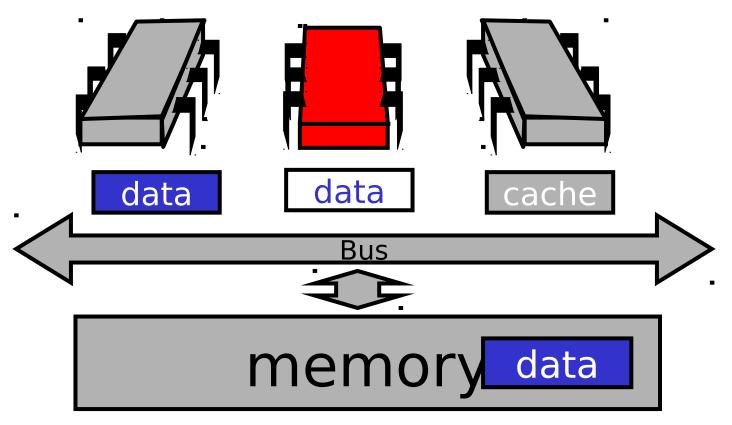


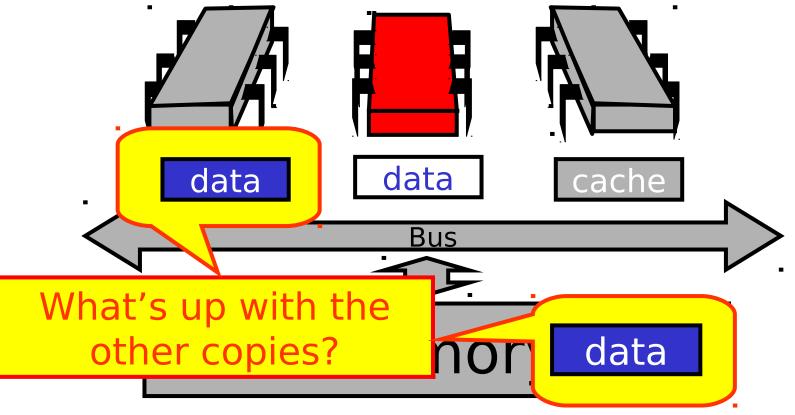
Other Processor Responds











Cache Coherence

- We have lots of copies of data
 - Original copy in memory
 - Cached copies at processors
- Some processor modifies its own copy
 - What do we do with the others?
 - How to avoid confusion?

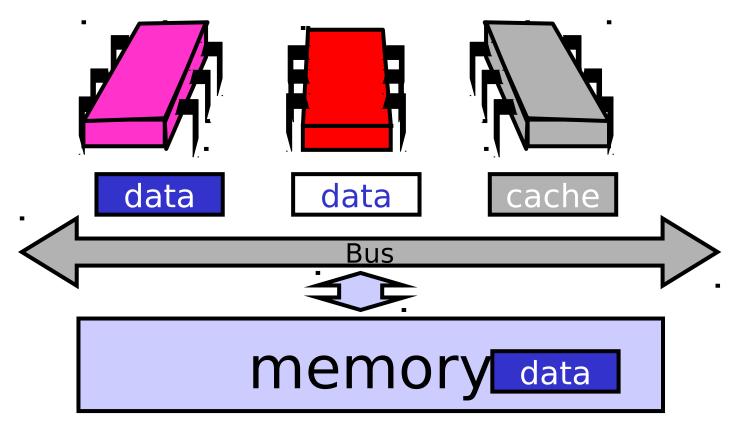
Write-Back Caches

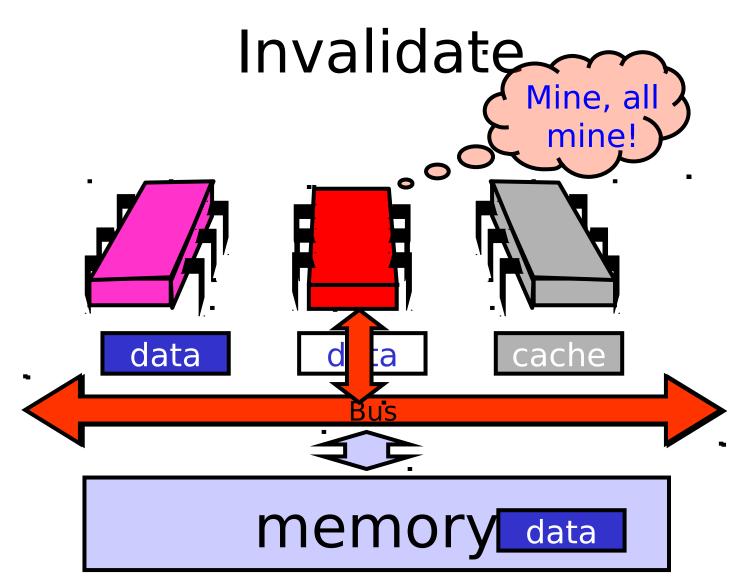
- Accumulate changes in cache
- Write back when needed
 - Need the cache for something else
 - Another processor wants it
- On first modification
 - Invalidate other entries
 - Requires non-trivial protocol ...

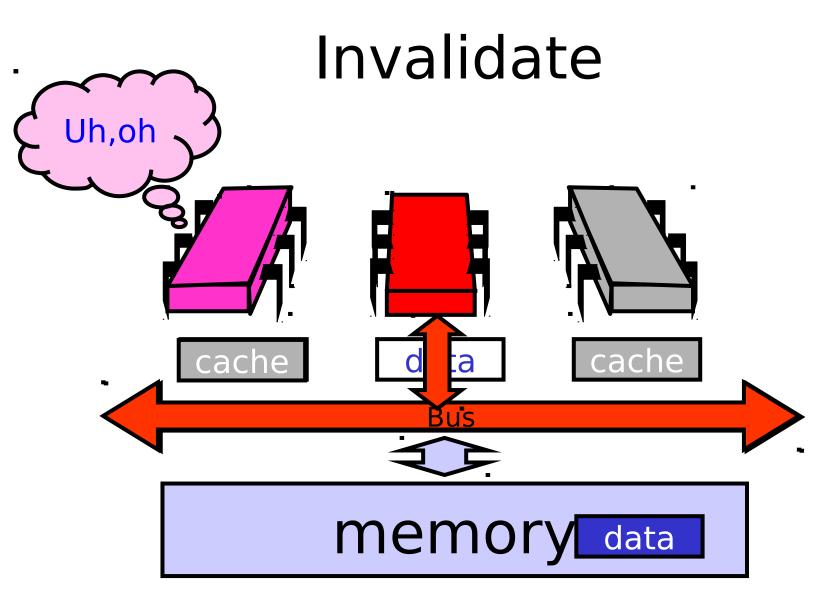
Write-Back Caches

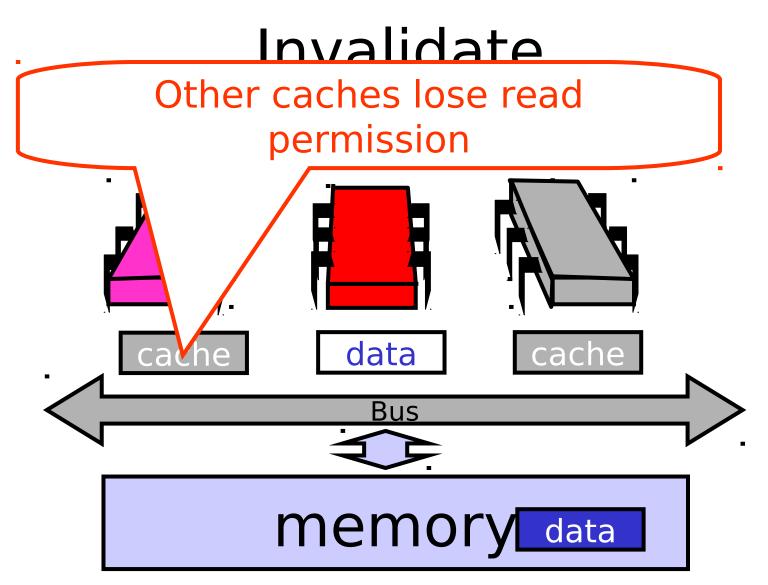
- Cache entry has three states
 - Invalid: contains raw seething bits
 - Valid: I can read but I can't write
 - Dirty: Data has been modified
 - Intercept other load requests
 - Write back to memory before using cache

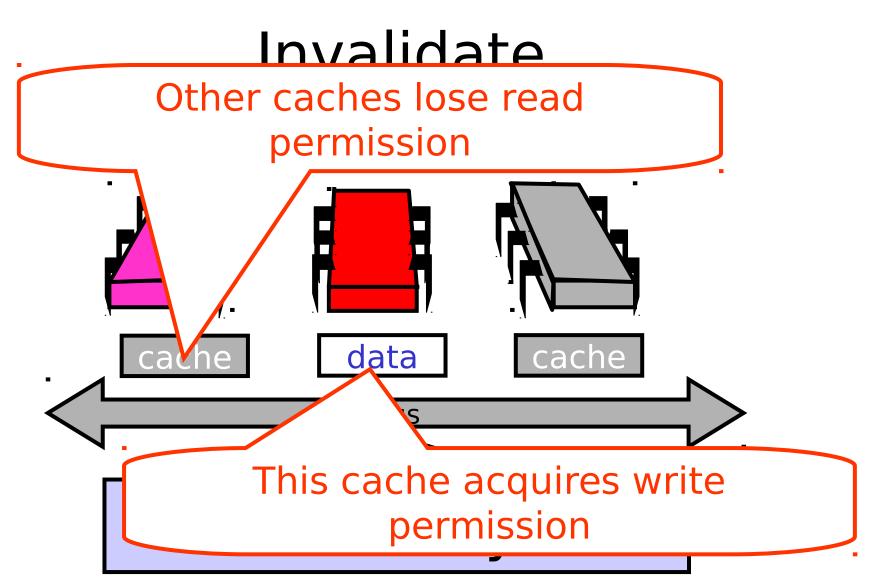
Invalidate



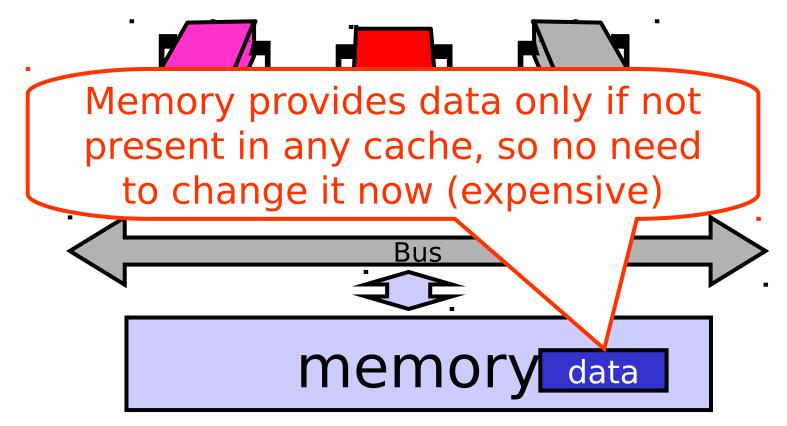




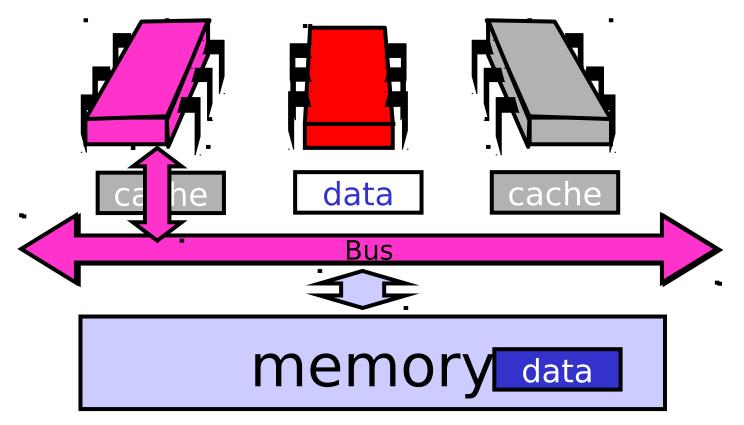


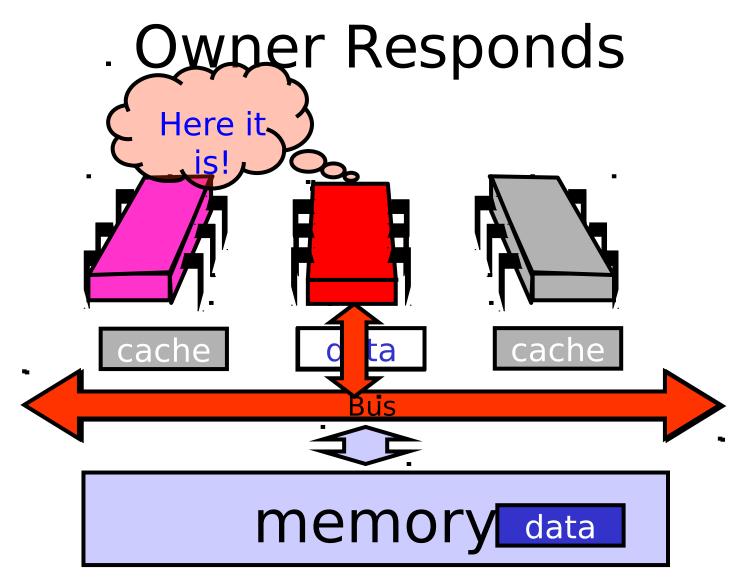


Invalidate

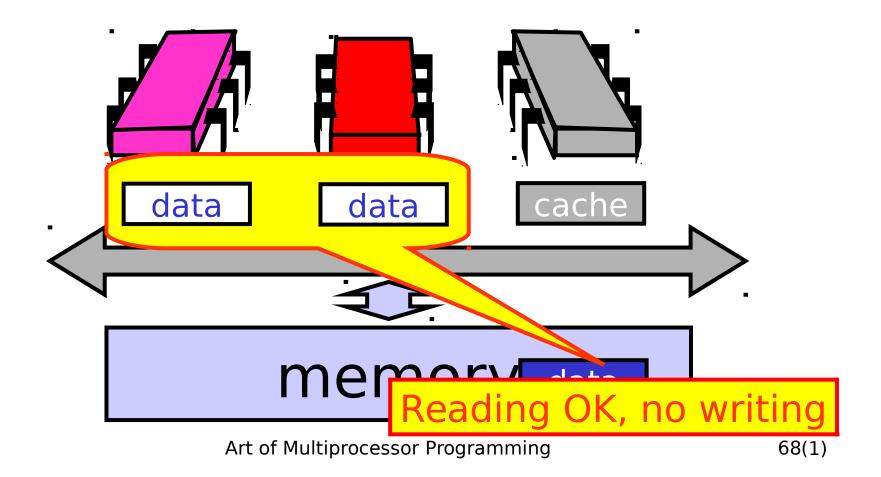


Another Processor Asks for Data





End of the Day ...



Mutual Exclusion

- What do we want to optimize?
 - Bus bandwidth used by spinning threads
 - Release/Acquire latency
 - Acquire latency for idle lock

Simple TASLock

- TAS invalidates cache lines
- Spinners
 - Miss in cache
 - Go to bus
- Thread wants to release lock
 delayed behind spinners

Test-and-test-and-set

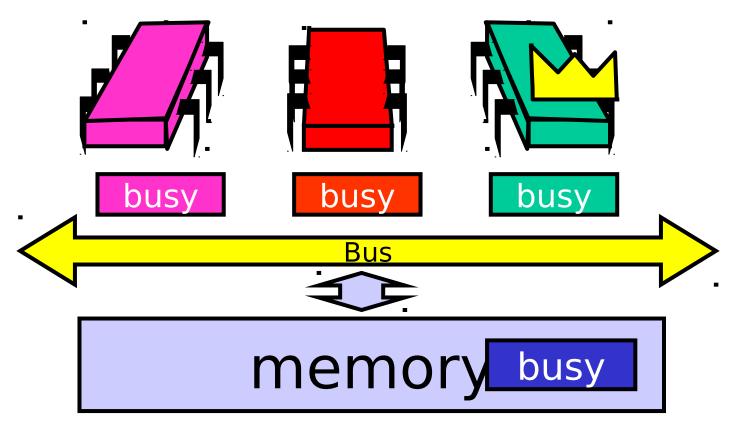
- Wait until lock "looks" free
 - Spin on local cache
 - No bus use while lock busy
- Problem: when lock is released

– Invalidation storm ...

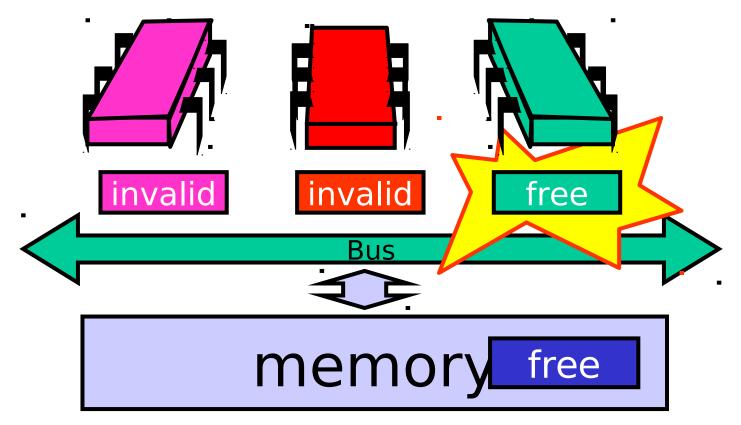
Test-and-test-and-set Lock

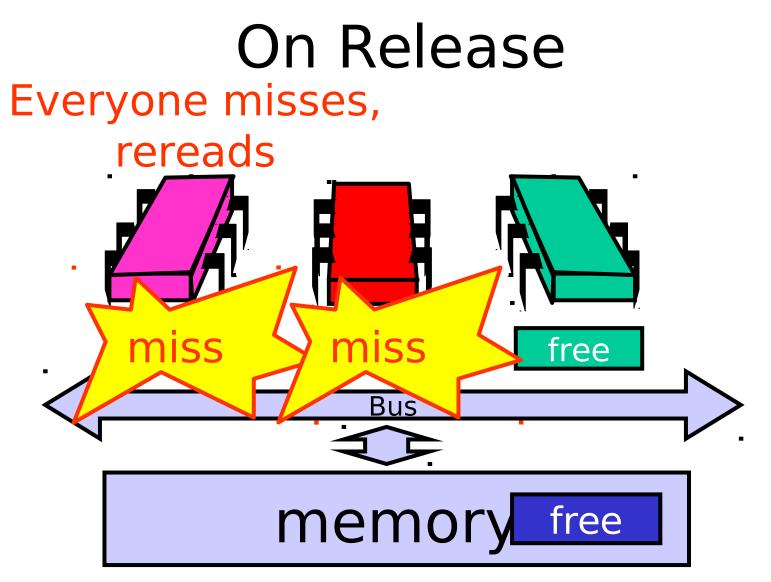
```
class TTASlock {
 AtomicBoolean state =
  new AtomicBoolean(false);
 void lock() {
  while (true) {
  while (state.get()) {}
   if (!state.getAndSet(true))
    return;
```

Local Spinning while Lock is Busy

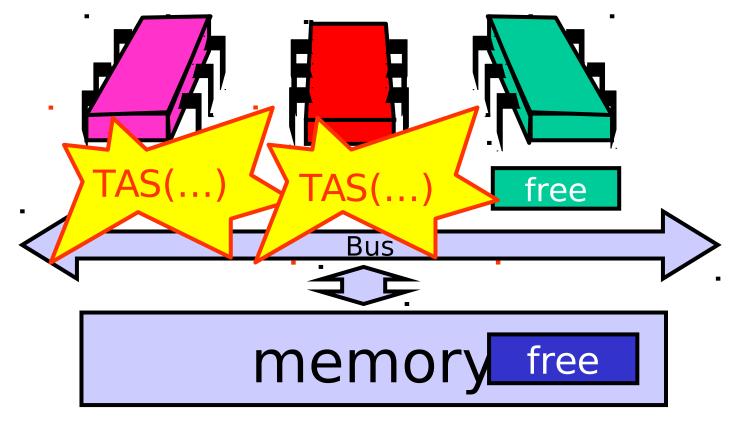


On Release





On Release Everyone tries TAS



Test-and-test-and-set Lock

```
class TTASlock {
 AtomicBoolean state =
  new AtomicBoolean(false);
 void lock() {
  while (true) {
  while (state.get()) {}
   if (!state.getAndSet(true))
    return;
```

Problems

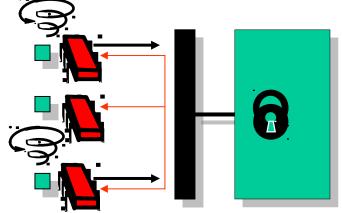
- Everyone misses

 Reads satisfied sequentially
- Everyone does TAS

 Invalidates others' caches
- Eventually quiesces after lock acquired
 - How long does this take?

Measuring Quiescence Time

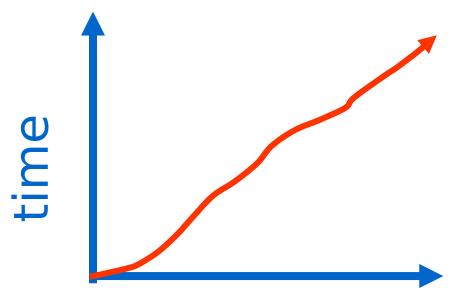
- X = time of ops that don't use the bus
- Y = time of ops that cause intensive bus traffic



In critical section, run ops X then ops Y. As long as Quiescence time is less than X, no drop in performance.

By gradually varying X, can determine the exact time to quiesce.

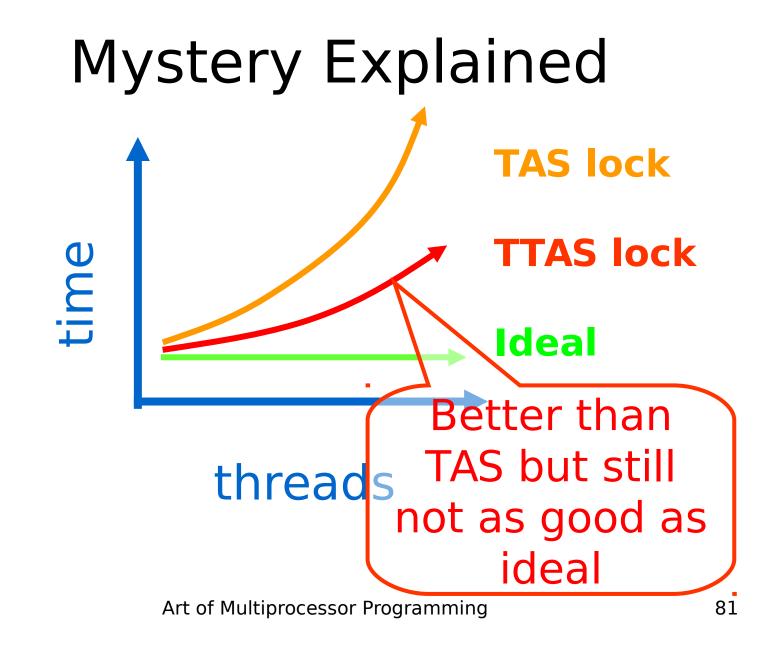
Quiescence Time



Increses linearly with the number of processors for bus architecture

threads

Art of Multiprocessor Programming

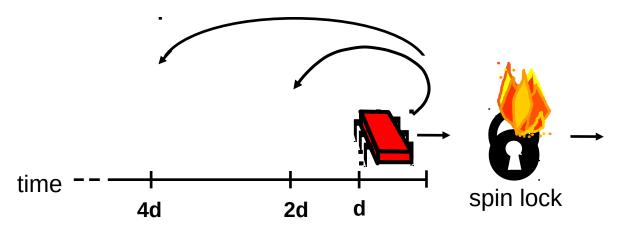


Solution: Introduce Delay

- If the lock looks free
 - But I fail to get it
- There must be lots of contention
 - Better to back off than to collide again

time -- $r_2d r_1d d$ - spin lock

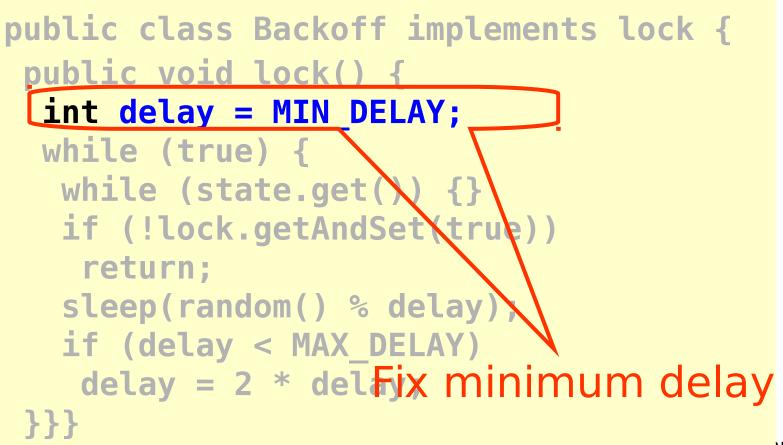
Dynamic Example: Exponential Backoff



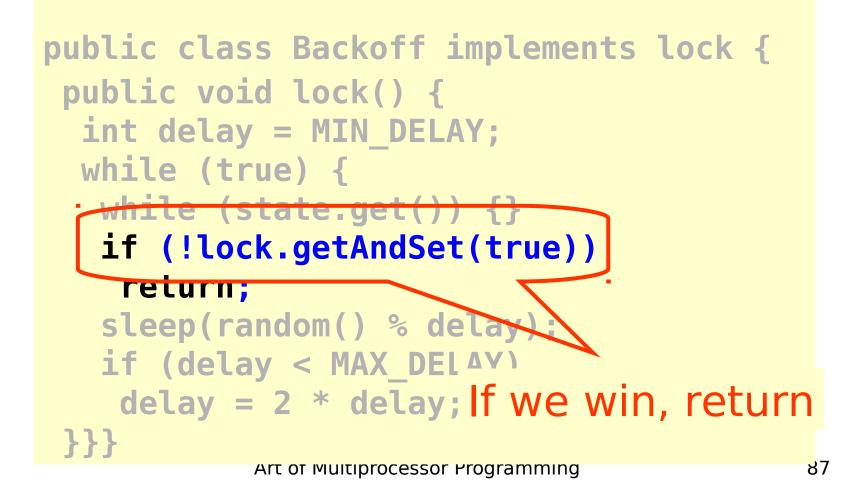
If I fail to get lock

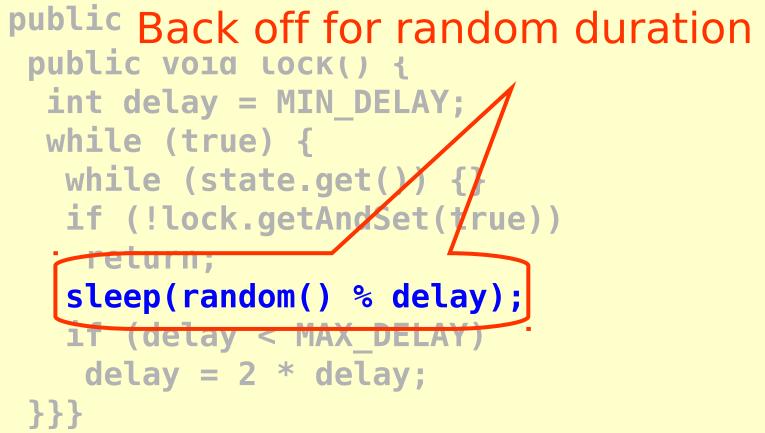
- wait random duration before retry
- Each subsequent failure doubles expected wait

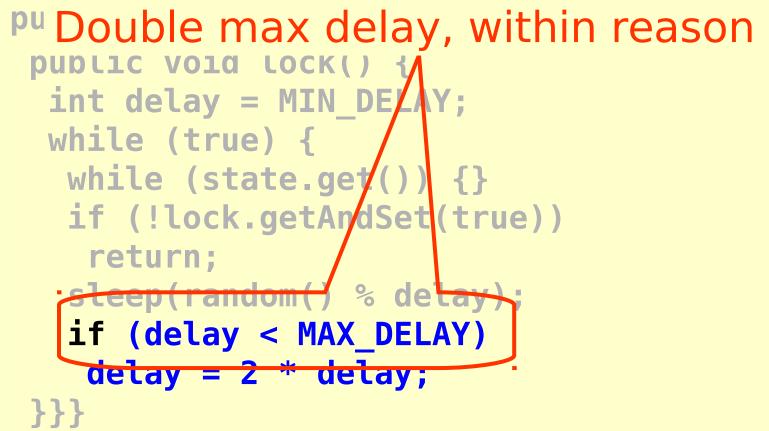
```
public class Backoff implements lock {
 public void lock() {
  int delay = MIN DELAY;
 while (true) {
  while (state.get()) {}
  if (!lock.getAndSet(true))
    return;
   sleep(random() % delay);
   if (delay < MAX DELAY)
    delay = 2 * delay;
}}
```



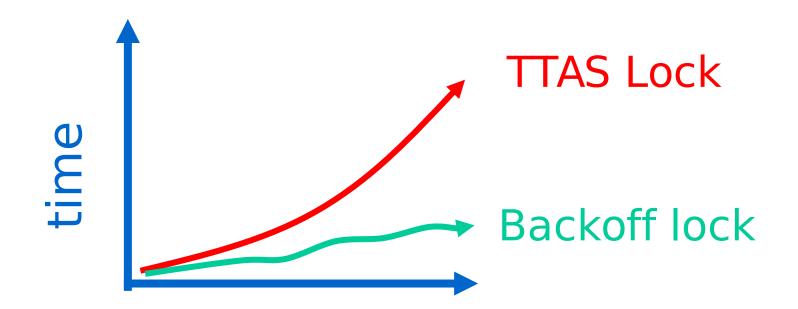
public class Backoff implements lock { public void lock() { int delay = MIN DELAY; while (true) { while (state.get()) {} if (!lock.getAndSet(true)) return; sleep(random() % delay if (delay < MAY DFIAY) delay = : Wait until lock looks free }}}







Spin-Waiting Overhead



threads

Art of Multiprocessor Programming

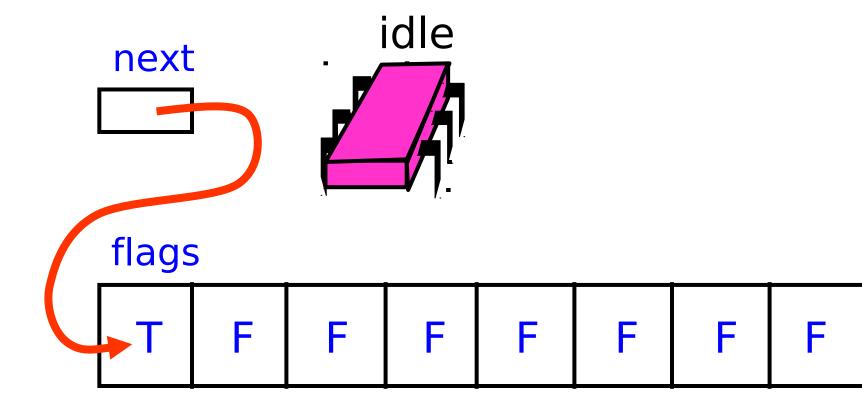
Backoff: Other Issues

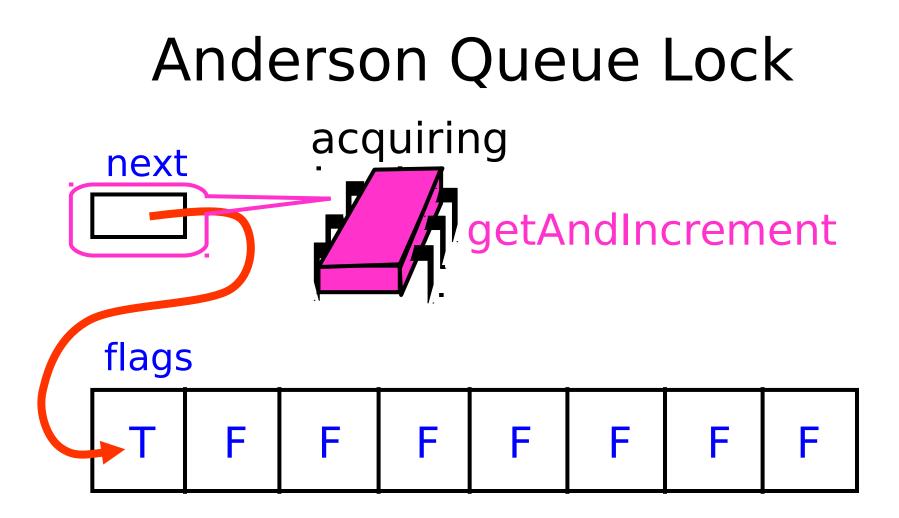
- Good
 - Easy to implement
 - Beats TTAS lock
- Bad
 - Must choose parameters carefully
 - Not portable across platforms

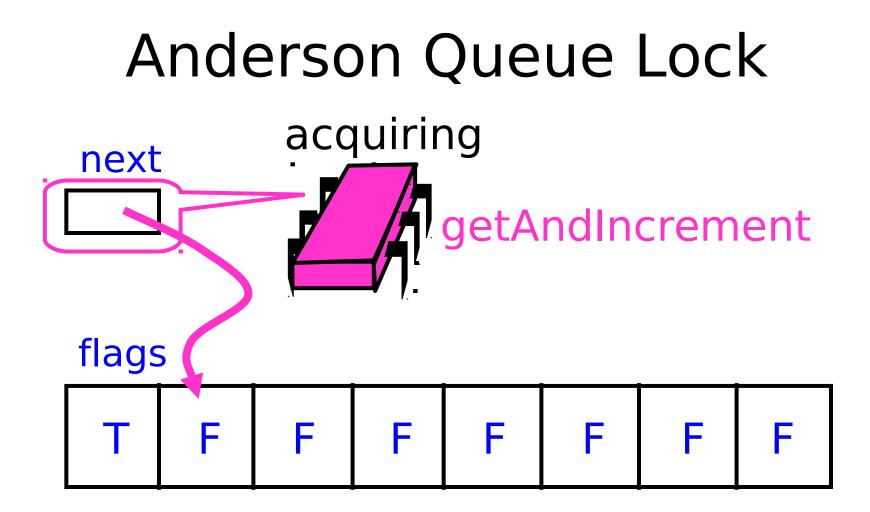
Idea

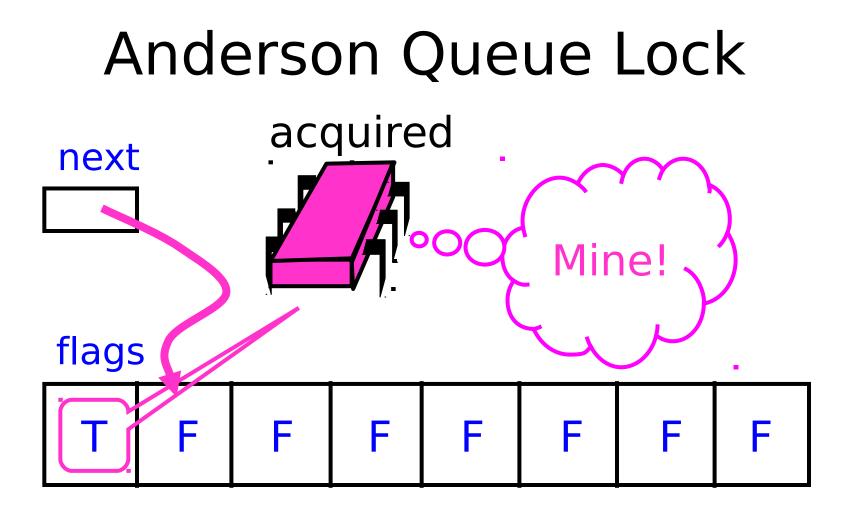
- Avoid useless invalidations

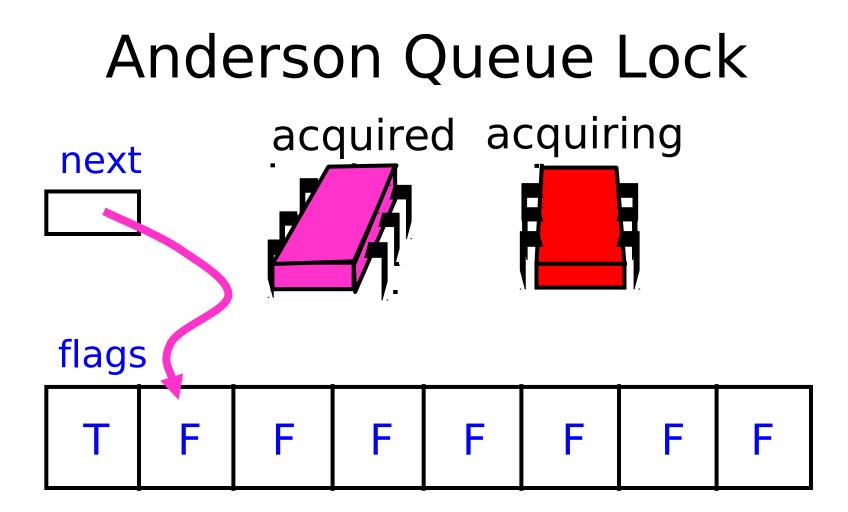
 By keeping a queue of threads
- Each thread
 - Notifies next in line
 - Without bothering the others

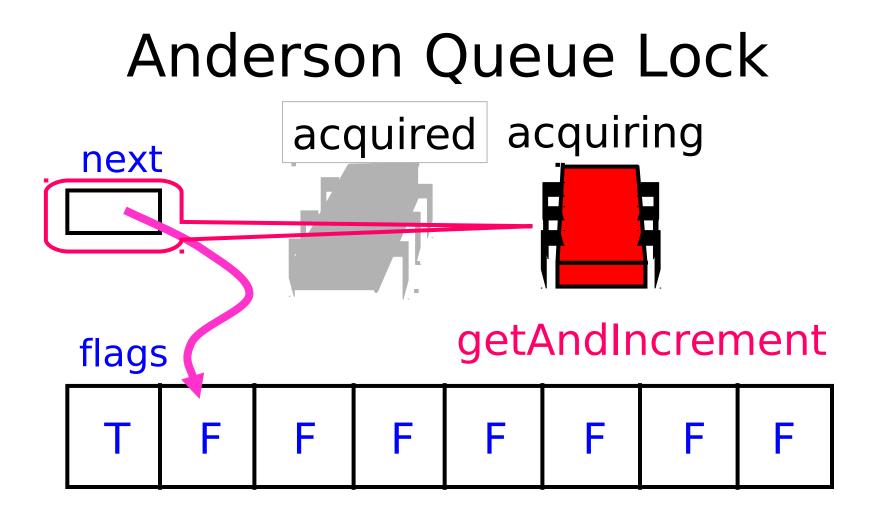


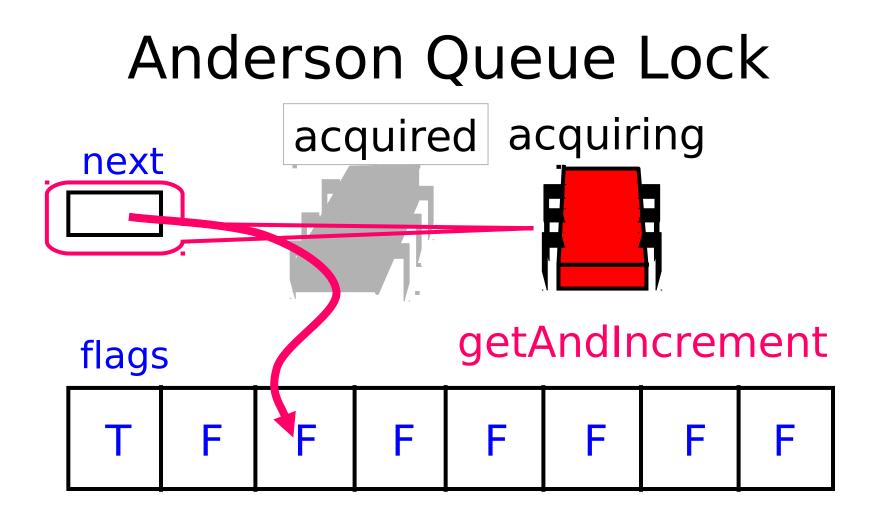


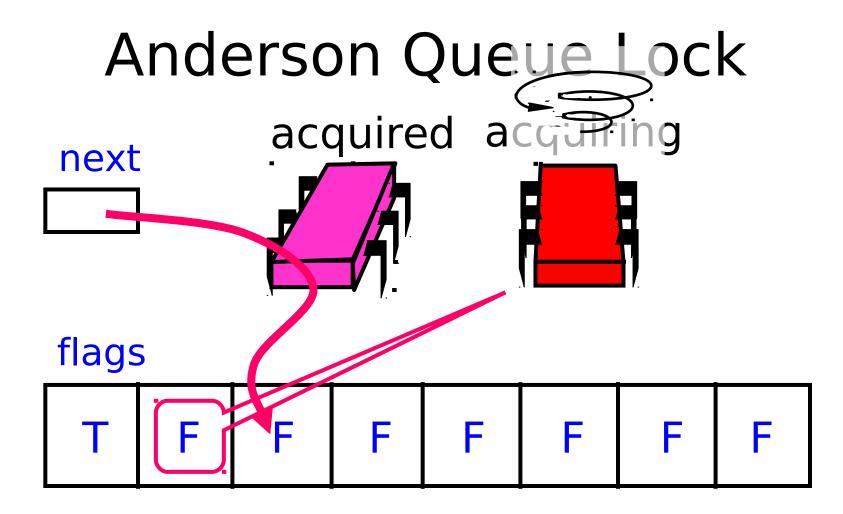


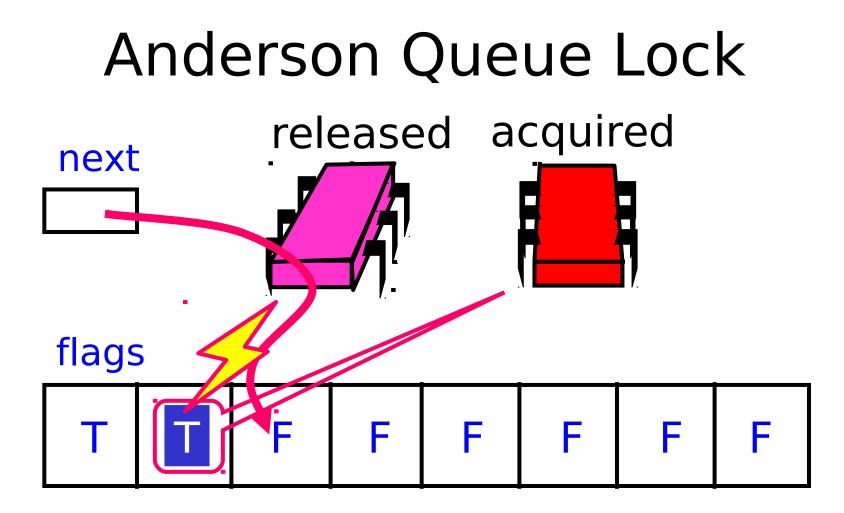


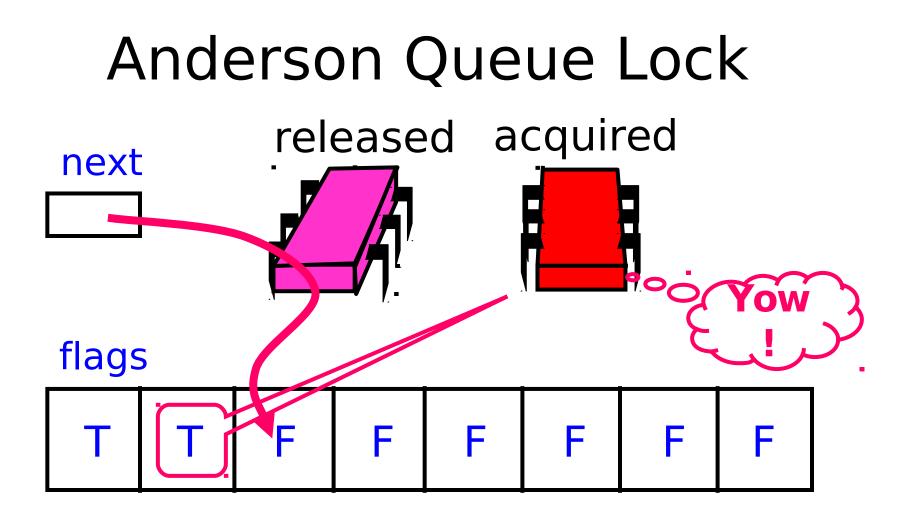






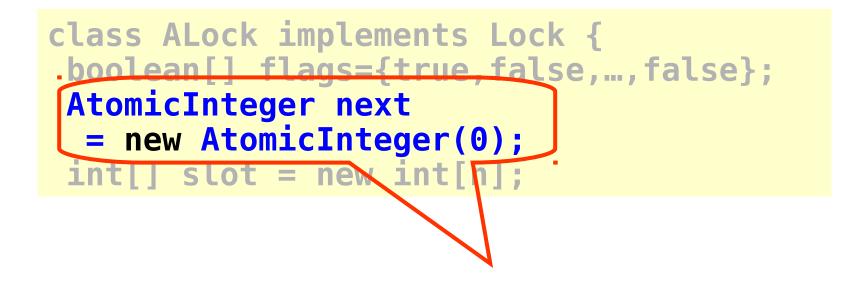




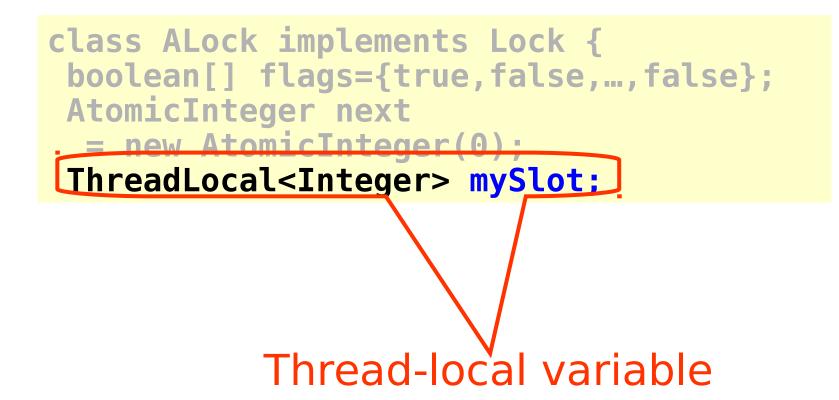


class ALock implements Lock {
 boolean[] flags={true,false,...,false};
 AtomicInteger next
 = new AtomicInteger(0);
 int[] slot = new int[n];

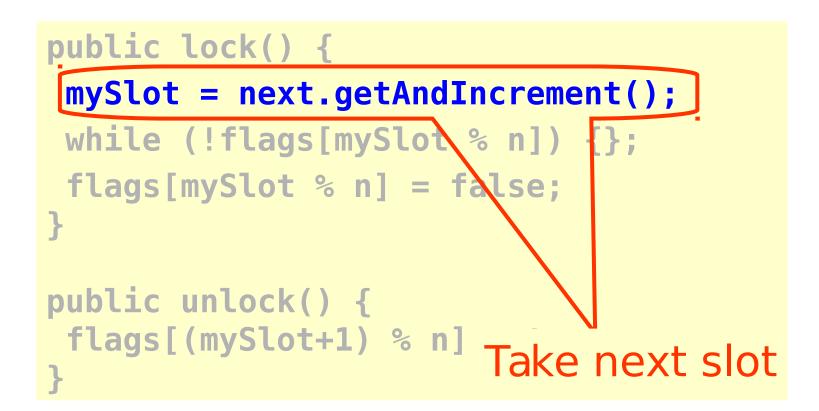
class ALock implements Lock { boolean[] flags={true, false,..., false}; AtomicInteger next = new AtomicInteger(0); int[] slot = new int[n]; One flag per thread

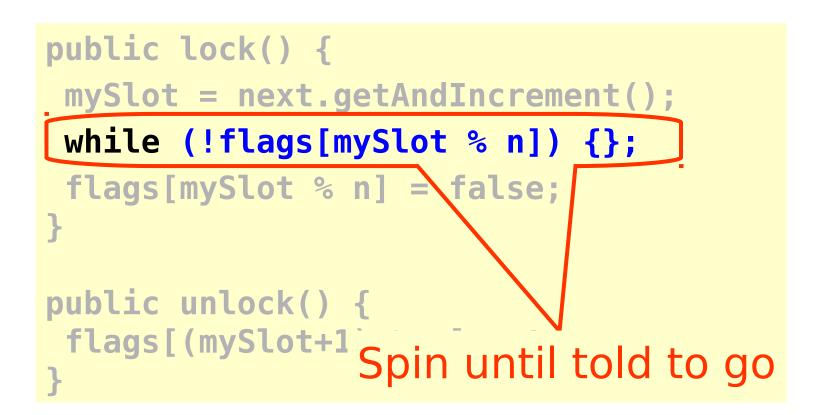


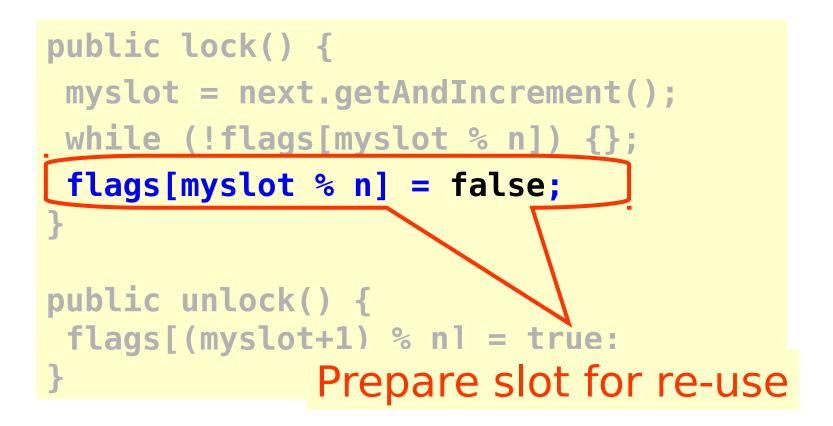
Next flag to use



```
public lock() {
mySlot = next.getAndIncrement();
while (!flags[mySlot % n]) {};
 flags[mySlot % n] = false;
}
public unlock() {
 flags[(mySlot+1) % n] = true;
}
```

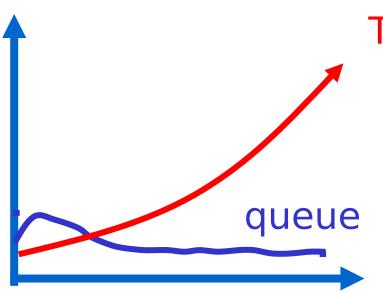






public lock() Tell next thread to go mySlot = next.getAndIncregent(); while (!flags[mySlot % {}; flags[mySlot % n] = fage <u>unlock</u>(flags[(mySlot+1) % n] = true;

Performance



TTAS

- Shorter handover than backoff
- Curve is practically flat
- Scalable performance
- FIFO fairness

• Good

- First truly scalable lock
- Simple, easy to implement
- Bad
 - Space hog
 - One bit per thread
 - Unknown number of threads?
 - Small number of actual contenders?

CLH Lock

- FIFO order
- Small, constant-size overhead per thread

See part 2



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